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SERIES O: SPECIFICATIONS OF MEASURING EQUIPMENT

Equipment for the measurement of digital and analogue/digital parameters

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General requirements for instrumentation for performance measurements on digital transmission equipment

ITU-T Recommendation O.150

(Previously "CCITT Recommendation")

ITU-T O-SERIES RECOMMENDATIONS

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FOREWORD

The ITU-T (Telecommunication Standardization Sector) is a permanent organ of the International Telecommunication Union (ITU). The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, March 1-12, 1993).

ITU-T Recommendation O.150 was revised by ITU-T Study Group 4 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 12th of May 1996.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

CONTENTS

SUMMARY

This Recommendation contains general requirements applicable to the O-Series Recommendations for instrumentation for performance measurements on digital transmission equipment.

KEYWORDS

Block sizes, block-oriented measurement, detection and clearance of Alarm Indication Signal (AIS), detection and clearance of Loss Of Signal (LOS), digital test sequences, performance measurements, pseudo-random test sequences; tester.

Recommendation O.150

GENERAL REQUIREMENTS FOR INSTRUMENTATION FOR PERFORMANCE MEASUREMENTS ON DIGITAL TRANSMISSION EQUIPMENT

(revised in 1996)

1 Scope

This Recommendation contains general requirements applicable to instrumentation for performance measurements on digital transmission equipment. Such equipment is specified in the O-Series Recommendations. This Recommendation is intended to give general guidance in connection with specific O-Series Recommendations and is a help in finding the right measurement conditions for different applications.

This Recommendation defines such items as digital (pseudo-random) test sequences, block sizes for error performance measurements and the criteria for the detection and clearance of loss of frame and of alarm indication signal.

2 References

The following Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation G.823 (1993), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[2] CCITT Recommendation O.153 (1992), *Basic parameters for the measurement of error performance at bit rates below the primary rate*.

[3] CCITT Recommendation O.152 (1992), *Measuring equipment for bit rates of 64 kbit/s and N × 64 kbit/s*.

[4] CCITT Recommendation O.151 (1992), *Error performance measuring equipment operating at the primary rate and above*.

[5] ITU-T Recommendation G.826 (1993), *Error performance parameters and objectives for international, constant bit rate digital paths at or above the primary rate*.

[6] ITU-T Recommendation G.704 (1995), *Synchronous frame structures used at 1544, 6312, 2048, 8488 and 44 736 kbit/s.*

[7] CCITT Recommendation G.752 (1988), *Characteristics of digital multiplex equipments based on a second order bit rate of 6312 kbit/s and using positive justification*.

[8] CCITT Recommendation G.751 (1988), *Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification.*

[9] CCITT Recommendation G.703 (1991), *Physical/electrical characteristics of hierarchical digital interfaces.*

[10] ITU-T Recommendation G.775 (1994), *Loss Of Signal (LOS) and Alarm Indication Signal (AIS) defect detection and clearance criteria*.

[11] American National Standard for telecommunications ANSI T1.107-1988, *Digital hierarchy formats specifications*.

[12] CCITT Recommendation G.743 (1988), *Second order digital multiplex equipment operating at 6312 kbit/s and using positive justification*.

[13] CCITT Recommendation G.742 (1988), *Second order digital multiplex equipment operating at 8448 kbit/s and using positive justification*.

[14] CCITT Recommendation G.755 (1988), *Digital multiplex equipment operating at 139 264 kbit/s and multiplexing three tributaries at 44 736 kbit/s*.

3 Standardized test sequences

Bit error measurements are important means to assess the performance of digital transmission equipment. So-called "true" bit error measurements, during which every error can be detected, can only be carried out if the bit sequence of the pattern used for the measurement is exactly known. Because of its random nature, this condition is normally not fulfilled by real traffic.

Therefore, it is necessary to specify reproducible test sequences which simulate real traffic as closely as possible. Reproducible test sequences are also a prerequisite to perform end-to-end measurements.

Pseudo-random sequences with a length of $2^n - 1$ bits are the most common answers to this problem. In addition to strings of n consecutive ZEROs (so-called inverted signal) and n – 1 consecutive ONEs, such sequences contain any possible combination of ZEROs and ONEs within a string length depending on n. (For the value of n see Clauses 4 and 5.)

Pseudo-random sequences of different lengths are specified in this Recommendation.

4 Properties of pseudo-random test sequences

The properties of a test sequence should meet the requirements of the system under test. In general, the length of a pseudo-random sequence shall increase with the bit rate at which measurements are performed. This avoids the sequence repetition frequency becoming too high which would not be in accordance with the situation found in practice.

Pseudo-random sequences may be produced by means of shift registers with appropriate feedback. If the shift register has n stages, the maximum sequence length will be $2^n - 1$ bits.

If the digital signal is directly taken from the output of the shift register (non-inverted signal) the longest string of consecutive ZEROs will be equal n – 1. If the signal is inverted, n consecutive ZEROs will be produced.

It is possible to generate pseudo-random sequences with these properties by other means than shift registers.

4.1 Measurements through scramblers

The unit under test may contain scramblers. This may yield unexpected measurement results if the value n as described in clause 4 has common integer multiples with the number of stages of the scrambler. To reduce the probability that this problem will occur, the value of n for test sequences specified more recently is a prime number.

4.2 Loss of sequence synchronization

Bit error measurements using pseudo-random sequences can only be performed if the reference sequence produced on the receiving side of the test set-up is correctly synchronized to the sequence coming from the object under test. In order to achieve compatible measurement results, it is necessary that the sequence synchronization characteristics are specified.

The following requirement is applicable to all O-Series Recommendations dealing with error performance measurements using pseudo-random sequences.

Sequence synchronization shall be considered to be lost and resynchronization shall be started if:

a) the bit error ratio is ≥ 0.20 during an integration interval of 1 second; or

b) it can be unambiguously identified that the test sequence and the reference sequence are out of phase.

NOTE – One method to recognize the out-of-phase condition is the evaluation of the error pattern resulting from the bit-by-bit comparison. If the error pattern has the same structure as the pseudo-random test sequence, the out-of-phase condition is reached.

4.3 "Framed" measurements

Certain measurements require that the test sequence is transmitted as "payload" within a valid frame.

In this case, transmission of the test sequence shall be stopped when the frame alignment signal is transmitted.

More detailed information is given in clause 6.

4.4 Jitter measurements

Digital test sequences are not only used in error measurements but also for measuring the jitter transfer function or tolerable input jitter. Special attention should be paid in this case to the length of the test sequence used in the measurement. If the sequence is too short (high sequence repetition frequency), the spectral distribution of the test signal may differ substantially from the properties of real traffic. In this case, the measurement results will not reflect the practical situation. See Annex A/G.823 [1] in this connection.

5 Digital test sequences used in the O-Series Recommendations

This clause describes the digital test sequences used in the O-Series Recommendations and their main applications. Table 1 gives a summary.

TABLE 1/O.150

Digital test sequences used in the O-Series Recommendations

Length of sequence (bits)	Consecutive zeros	Used in Rec.	Use of sequence
$2^{09} - 1$	8	O.153	Error measurements on data circuits at bit rates up to 14 400 bit/s
$2^{11} - 1$	10	O.152	Error and jitter measurements at bit rates of 64 kbit/s and N × 64 kbit/s
$2^{15} - 1$	15	O.151	Error and jitter measurements at bit rates of 1544, 2048, 6312, 8448, 32 064 and 44 736 kbit/s
$2^{20} - 1$	19	O.153	Error measurements on data circuits at bit rates up to 72 kbit/s
$2^{20} - 1$	14	O.151	Error and jitter measurements at bit rates of 1544, 6312, 32 064 and 44 736 kbit/s
$2^{23} - 1$	23	O.151	Error and jitter measurements at bit rates of 34 368 and 139 264 kbit/s
$2^{29} - 1$	29	–	Specific measurement tasks
$2^{31} - 1$	31	–	Specific measurement tasks

5.1 511-bit pseudo-random test sequence

This sequence is primarily intended for error measurements on data circuits at bit rates up to 14 400 bit/s (see Recommendation O.153 [2]).

The sequence may be generated in a nine-stage shift register whose 5th and 9th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. The sequence begins with the first ONE of 9 consecutive ONEs.

- Number of shift register stages 9
- Length of pseudo-random sequence $2^9 - 1 = 511$ bits
- Longest sequence of zeros 8 (non-inverted signal)

5.2 2047-bit pseudo-random test sequence

This sequence is primarily intended for error and jitter measurements on circuits operating at bit rates of 64 kbit/s and $N \times 64$ kbit/s (see Recommendations O.152 [3] and O.153 [2]).

The sequence may be generated in an eleven-stage shift register whose 9th and 11th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

- Number of shift register stages 11
- Length of pseudo-random sequence $2^{11} - 1 = 2047$ bits
- Longest sequence of zeros 10 (non-inverted signal)

NOTES

1 When performing measurements at a bit rate of $N \times 64$ kbit/s, consecutive 8-bit-blocks of the test sequence shall be transmitted in consecutive time slots. The beginning of the pseudo-random test sequence need not be related to the frame repetition rate.

2 Whether N can be any number between 1 and 31 requires further study.

5.3 32 767-bit pseudo-random test sequence

This sequence is primarily intended for error and jitter measurements at bit rates of 1544, 2048, 6312, 8448, 32 064 and 44 736 kbit/s (see Recommendation O.151 [4]).

The sequence may be generated in a fifteen-stage shift register whose 14th and 15th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

- Number of shift register stages 15
- Length of pseudo-random sequence $2^{15} - 1 = 32\,767$ bits
- Longest sequence of zeros 15 (inverted signal)

5.4 1 048 575-bit pseudo-random test sequence

This sequence is primarily intended for error measurements on data circuits at bit rates up to 72 kbit/s (see Recommendation O.153 [2]).

The sequence may be generated in a twenty-stage shift register whose 3rd and 20th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

- Number of shift register stages 20
- Length of pseudo-random sequence $2^{20} - 1 = 1\,048\,575$ bits
- Longest sequence of zeros 19 (non-inverted signal)

NOTE – The two test sequences of length $2^{20} - 1$ bits described in 5.4 and 5.5 are not identical because a different feedback is employed if the sequence is produced by means of a shift register. The sequence specified in 5.5 suppresses consecutive sequences of more than 14 zeros.

5.5 1 048 575-bit pseudo-random test sequence with zero suppression

This sequence is primarily intended for error and jitter measurements at bit rates of 1544, 6312, 32 064 and 44 736 kbit/s (see Recommendation O.151 [4]).

The sequence may be generated in a twenty-stage shift register whose 17th and 20th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. An output bit is forced to be a ONE whenever the next 14 bits are all ZERO.

- Number of shift register stages 20
- Length of pseudo-random sequence $2^{20} - 1 = 1\,048\,575$ bits
- Longest sequence of zeros 14 (see Note)

This pseudo-random sequence satisfies the following:

$$Q_{n+1}(k + 1) = Q_n(k),\ n = 1, 2, ..., 19,$$

$$Q_1(k + 1) = Q_{17}(k) \oplus Q_{20}(k), \text{ and}$$

$$RD(k) = Q_{20}(k) + \overline{Q_6(k) + . . . + Q_6(k)}$$

where:

$Q_n(k)$	Present state of n-th stage
$Q_n(k + 1)$	Next state of n-th stage
$RD(k)$	Present value of output
+	A logic OR operation
$\oplus$	A logic EXCLUSIVE OR operation
$\overline{\ \ }$	A logic NEGATION operation

NOTE – The two test sequences of length $2^{20} - 1$ bits described in 5.4 and 5.5 are not identical because a different feedback is employed if the sequence is produced by means of a shift register. The sequence specified in this subclause suppresses consecutive sequences of more than 14 zeros.

5.6 8 388 607-bit pseudo-random test sequence

This sequence is primarily intended for error and jitter measurements at bit rates of 34 368, 44 736 and 139 264 kbit/s (see Recommendation O.151 [4]).

The sequence may be generated in a twenty-three-stage shift register whose 18th and 23rd stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

- Number of shift register stages 23
- Length of pseudo-random sequence $2^{23} - 1 = 8\ 388\ 607$ bits
- Longest sequence of zeros 23 (inverted signal)

5.7 536 870 911-bit pseudo-random test sequence

This sequence may be used for special measurement tasks, e.g., delay measurements at higher bit rates. If error performance measurements require longer sequences, future studies shall take into account this sequence.

The sequence may be generated in a twenty-nine-stage shift register whose 27th and 29th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

- Number of shift register stages 29
- Length of pseudo-random sequence $2^{29} - 1 = 536\ 870\ 911$ bits
- Longest sequence of zeros 29 (inverted signal)

5.8 2 147 483 647-bit pseudo-random test sequence

This sequence may be used for special measurement tasks, e.g. delay measurements at higher bit rates. If error performance measurements require longer sequences, future studies shall take into account this sequence.

The sequence may be generated in a twenty-nine-stage shift register whose 28th and 31st stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

- Number of shift register stages 31
- Length of pseudo-random sequence $2^{31} - 1 = 2\ 147\ 483\ 647$ bits
- Longest sequence of zeros 31 (inverted signal)

6 Description of framed test sequences at different bit rates

6.1 General

Certain test objects require specific bit sequences at their input to operate correctly. Typical examples of such devices are digital demultiplexers which need a test signal containing at least the correct frame alignment signal. Additional information, e.g. parity bits, alarm bits may need to be set to a defined state.

6.1.1 Testing digital demultiplexers

Here, two cases have to be considered:

In the general case, measurements shall be performed through a digital demultiplexer and a correctly structured test signal is required. This signal shall contain the appropriate frame alignment word, stuffing (justification) bits and all required path overhead bits to provide proper operation of the path termination. Thus, the test signal should be structured as it would appear at the output of a correctly operating digital multiplexer. This structure is shown in the following example.

One Frame							
Set 1		Set 2		Set 3		Set 4	
FAS	TS 1, TS 2, TS 3, TS 4	C_{j1}	TS 1, TS 2, TS 3, TS 4	C_{j2}	TS 1, TS 2, TS 3, TS 4	C_{j3}	TS 1, TS 2, TS 3, TS 4
FAS Frame Alignment Signal plus Alarm Bits TS m Interleaved Test Sequence Bits from Tributaries 1 to 4 C_{jn} Justification Control Bits							

NOTE – Detailed information on multiplex structures is given in 6.4 to 6.10. In these subclauses, test sequence bits are numbered consecutively. This does not mean that these bits shall belong to the same sequence. Depending on the application, it may be preferable to provide independent test sequences in the sets representing the lower order tributaries.

In the second case, only the behaviour of the input sections of a demultiplexer shall be tested. Examples of such tests are the measurement of tolerable input jitter, framing tests, indication of alarms, etc. For this type of measurement, the test signal is not required to contain the correct stuffing information, nor is it necessary to structure the higher order digital input signal in such a way that meaningful digital signals appear at the tributary outputs. Such a signal is structured as shown below.

Frame 1		Frame 2		Frame 3		.....	Frame n	
FAS	TS 1 to u	FAS	TS u + 1 to v	FAS	TS v + 1 to w	.....	FAS	TS x + 1 to y
FAS Frame Alignment Signal plus Alarm Bits TS 1 to TS y Test Sequence Bits which may belong to one sequence								

6.2 Digital frames operating at bit rates of 1544 kbit/s

With regard to these frames see Recommendation G.704 [6] and ANSI T1.107-1988 [11].

6.2.1 12-Frame multiframe or superframe

A superframe comprises 12 frames (Fr 01-Fr 12), consists of 2316 bits and is structured as follows:

Fr 01	Fr 02	Fr 03	Fr 04	Fr 05	Fr 06	Fr 07	Fr 08	Fr 09	Fr 10	Fr 11	Fr 12

In frames Fr 01 to Fr 05 and frames Fr 07 to Fr 11, the frame structure shall be as follows:

Bit 1	Bits 2-193
Frame Bit	Test Sequence

In frames Fr 06 and Fr 12 the frame structure shall be as follows:

Bit 1	Bit 2-8	Bit 9	Bits 10-16	Bit 17	Bits 18-24	Bit 25	.....	Bits 186-192	Bit 193
Frame Bit	TS 1-7	a1	TS 8-14	a2	TS 15-21	a3	.....	TS 162-168	a24

NOTE – Twelve frame overhead bits occupy sequential frame overhead bit positions (bit 1) as follows: F1, S1, F2, S2, F3, S4, F5, S5, F6, S6 where F bits represent the Frame Alignment Signal and S bits the Multiframe Alignment Signal.

TS = Test Sequence Bits;

aN = Signalling bit for channel N.

Frame 12 may contain either a or b signalling bits depending on selection of two or four state signalling. In the transparent mode (64 kbit/s) a bits are used for test sequence bits. Therefore, frames 06 and 12 contain the test sequence in bit positions 2-193.

6.2.2 24-Frame multiframe or extended superframe

An extended superframe comprises 24 frames (Fr 01-Fr 24), consists of 4632 bits and is structured as follows:

Fr 01	Fr 02	Fr 03	Fr 04	Fr 05	Fr 06	.....	.....	.....	Fr 22	Fr 23	Fr 24

In frames Fr 01 to Fr 05, Fr 07 to Fr 11, Fr 13 to 17 and Fr 19 to 23, the frame structure shall be as follows:

Bit 1	Bits 2-193
Frame Bit	Test Sequence

In frames Fr 06, Fr 12, Fr 18 and Fr 24, the frame structure shall be as follows:

Bit 1	Bit 2-8	Bit 9	Bits 10-16	Bit 17	Bits 18-24	Bit 25	.....	Bits 186-192	Bit 193
Frame Bit	TS 1-7	s1	TS 8-14	s2	TS 15-21	s3	.....	TS 162-168	s24

NOTE – Twenty-four frame overhead bits occupy sequential frame overhead bit positions (bit 1) as follows: M1, C1, M2, F1, M3, C2, M4, F2, M5, C3, M6, F3, M7, C4, M8, F4, M9, C5, M10, F5, M11, C6, M12, F6 where F bits represent the Frame Alignment Signal and M bits a data link. C bits are the CRC-6 bits.

The meaning of the signalling bits (s bits):

Frame 06: s = a, Frame 12: s = a or b, Frame 18: s = a or c, Frame 24: s = a, b or d dependent on selection of two, four or sixteen state signalling.

TS = Test Sequence Bits.

In the transparent mode (64 kbit/s) s bits are used for test sequence bits. Therefore, frame 06, frame 12, frame 18 and frame 24 contain the test sequence in bit positions 2-193.

6.3 Digital frames operating at bit rates of 2048 kbit/s

With regard to these frames see Recommendation G.704 [6].

6.3.1 Frames without CRC-4 procedure and providing common channel signalling

In this case, the frame structure shall be as follows:

Time Slot 0	Time Slots 1-15	Time Slot 16	Time Slots 17-31
1001 1011	Test Sequence	Test Sequence	Test Sequence
11AS SSSS	Test Sequence	Test Sequence	Test Sequence
A Remote alarm indication S Spare bits			

6.3.2 Frames without CRC-4 procedure and providing channel associated signalling

In this case, the frame structure shall be as follows:

Time Slot 0	Time Slots 1-15	Time Slot 16	Time Slots 17-31
1001 1011	Test Sequence	abcd abcd	Test Sequence
11AS SSSS	Test Sequence	abcd abcd	Test Sequence
A Remote alarm indication S Spare bits a, b, c, d Signalling bits			

6.3.3 Frames with CRC-4 procedure and providing channel associated signalling

In this case, the frame structure shall be as follows:

Time Slot 0	Time Slots 1-15	Time Slot 16	Time Slots 17-31
C001 1011	Test Sequence	abcd abcd	Test Sequence
C1AS SSSS	Test Sequence	abcd abcd	Test Sequence
C Cyclic redundancy check bit (CRC-4) A Remote alarm indication S Spares bits a, b, c, d Signalling bits			

6.4 Digital frames operating at bit rates of 6312 kbit/s

In this case, the frame structure shall be as follows (see Recommendation G.743 [12] and ANSI T1.107-1988 [11]):

A multiframe (M-frame) comprises four M-subframes of 294 bits each and has a length of 1176 bits.

Subframe 1		Subframe 2		Subframe 3		Subframe 4	
M1	293 bits	M2	293 bits	M3	293 bits	x	293 bits

The structure of the first M-subframe of 294 bits length is as follows:

Set 1		Set 2		Set 3		Set 4		Set 5		Set 6 (Stuff Block)	
Bit 1	Bits 2-49	Bit 50	Bits 51-98	Bit 99	Bits 100-147	Bit 148	Bits 149-196	Bit 197	Bits 198-245	Bit 246	Bits 247-294
M1	TS 1-48	C1	TS 49-96	F1	TS 97-144	C2	TS 145-192	C3	TS 193-240	F2	TS 241-288

M-Frame overhead bit sequence:

24 overhead bits occupy sequential overhead bit positions as follows:	M-Frame Frame Alignment Signal: M1 = 0, M2 = 1, M3 = 1
M1, C1, F1, C2, C3, F2,	M-Subframe Frame Alignment Signal: F1 = 0, F2 = 1
M2, C1, F1, C2, C3, F2,	x may be used as an alarm service digit.
M3, C1, F1, C2, C3, F2,	C1, C2 and C3 are stuffing control bits. C1 = C2 = C3 = 0 indicates no stuffing.
x, C1, F1, C2, C3, F2,	TS = Test Sequence Bits

The Stuff (justification) Block is structured as follows:

M1-Subframe	F2	Stuff bit 1	TS 242	TS 243	TS 244	TS 245	.....	TS 288
M2-Subframe	F2	TS 241	Stuff bit 2	TS 243	TS 244	TS 245	.....	TS 288
M3-Subframe	F2	TS 241	TS 242	Stuff bit 3	TS 244	TS 245	.....	TS 288
M4-Subframe	F2	TS 241	TS 242	TS 243	Stuff bit 4	TS 245	.....	TS 288
	NOTE – Concerning the use of stuffing (justification) bits see 6.1.1.							

6.5 Digital frames operating at bit rates of 8448 kbit/s

In this case, the frame structure shall be as follows (see Recommendation G.742 [13]):

A frame comprises four sets of 212 bits each and has a length of 848 bits.

Set 1		Set 2		Set 3		Set 4	
O1	200 bits	O2	208 bits	O3	208 bits	O4	208 bits

The detailed structure of sets 1 to 4 is given below.

	Overhead (O-) bits	Test Sequence Bits
Set 1	Frame Alignment Signal (bits 1 to 10) 1 1 1 1 0 1 0 0 0 0 Remote Alarm Indication (bit 11) Reserved for national use (bit 12)	Test Sequence Bits 1-200
Set 2	Justification control bits: C_{11}, C_{21}, C_{31}, C_{41}	Test Sequence Bits 201-408
Set 3	Justification control bits: C_{12}, C_{22}, C_{32}, C_{42}	Test Sequence Bits 409-616
Set 4	Justification control bits: C_{13}, C_{23}, C_{33}, C_{43} Bits from tributaries available for justification (bits 5-8)	Test Sequence Bits 617-824 (820)
NOTE – Concerning the use of stuffing (justification) bits see 6.1.1.		

6.6 Digital frames operating at bit rates of 32 064 kbit/s

In this case, the frame structure shall be as follows (see Recommendation G.752 [7]):

An M-frame comprises six sets (M-subframes) of 320 bits each and has a length of 1920 bits.

Set 1		Set 2		Set 3		Set 4		Set 5		Set 6	
M1	315 bits	M2	315 bits	M3	315 bits	M4	315 bits	M5	315 bits	M6	315 bits

The detailed structure of sets 1 to 6 is given below.

	M bits (bits 1-5)	Bits 6-320
Set 1	Frame Alignment Signal 1 1 0 1 0: (bits 1-5) $F_{11} = 1$, $F_{12} = 1$, $F_{13} = 0$, $F_{14} = 1$, $F_{15} = 0$	Test Sequence Bits 1-315
Set 2	Justification control bits: C_{11}, C_{21}, C_{31}, C_{41}, C_{51}	Test Sequence Bits 316-630
Set 3	Justification control bits: C_{12}, C_{22}, C_{32}, C_{42}, C_{52}	Test Sequence Bits 631-945
Set 4	Frame Alignment Signal 0 0 1 0 1: (bits 1-5) $F_{21} = 0$, $F_{22} = 0$, $F_{23} = 1$, $F_{24} = 0$, $F_{25} = 1$	Test Sequence Bits 946-1260
Set 5	Justification control bits: C_{13}, C_{23}, C_{33}, C_{43}, C_{53}	Test Sequence Bits 1261-1575
Set 6	Auxiliary bits H_1 to H_5 (Remote Alarm Indication)	Test Sequence Bits 1576-1890 (1885)
NOTE – The bit available for the justification of each tributary is the first slot of the tributary in set 6.		

6.7 Digital frames operating at bit rates of 34 368 kbit/s

In this case, the frame structure shall be as follows (see Recommendation G.751 [8]):

A frame comprises four sets of 384 bits each and has a length of 1536 bits.

Set 1		Set 2		Set 3		Set 4	
O1	372 bits	O2	380 bits	O3	380 bits	O4	388 bits

The detailed structure of sets 1 to 4 is given below.

	Overhead (O-) bits	Test Sequence Bits
Set 1	Frame Alignment Signal (bits 1 to 10) 1 1 1 1 0 1 0 0 0 0 Remote Alarm Indication (bit 11) Reserved for national use (bit 12)	Test Sequence Bits 1-372
Set 2	Justification control bits: C_{11}, C_{21}, C_{31}, C_{41}	Test Sequence Bits 373-752
Set 3	Justification control bits: C_{12}, C_{22}, C_{32}, C_{42}	Test Sequence Bits 753-1132
Set 4	Justification control bits: C_{13}, C_{23}, C_{33}, C_{43} Bits from tributaries available for justification (bits 5-8)	Test Sequence Bits 1133-1512 (1508)
NOTE – Concerning the use of stuffing (justification) bits see 6.1.1.		

6.8 Digital frames operating at bit rates of 44 736 kbit/s

In this case, the frame structure shall be as follows (see Recommendation G.752 [7] and ANSI T1.107-1988 [11]):

An M-frame comprises seven M-subframes of 680 bits each and has a length of 4760 bits.

Subframe 1		Subframe 2		Subframe 3		Subframe 4		Subframe 5		Subframe 6		Subframe 7	
X1	697 bits	X2	697 bits	P1	697 bits	P2	697 bits	M1	697 bits	M2	697 bits	M3	697 bits

The structure of the first M-subframe of 680 bits length is as follows:

Set 1		Set 2		Set 3		Set 4		Set 5		Set 6		Set 7		Set 8 (Stuff block)	
Bit 1	Bits 2-85	Bit 86	Bits 87-170	Bit 171	Bits 172-255	Bit 256	Bits 257-340	Bit 341	Bits 342-425	Bit 426	Bits 427-510	Bit 511	Bits 512-595	Bit 596	Bits 597-680
X1	TS 1-84	F1	TS 85-168	C1	TS 169-252	F2	TS 253-336	C2	TS 337-420	F3	TS 421-504	C3	TS 505-588	F4	TS 589-672

M-Frame overhead bit sequence:

56 overhead bits occupy sequential overhead bit positions as follows:

M-Frame Frame Alignment Signal:
M1 = 0, M2 = 1, M3 = 0

X1, F1, C1, F2, C2, F3, C3, F4,

M-Subframe Frame Alignment Signal:
F1 = 1, F2 = 0, F3 = 0, F4 = 1

X2, F1, C1, F2, C2, F3, C3, F4,

P1, F1, C1, F2, C2, F3, C3, F4,

In the multiplex application, stuffing for the n 6312 kbit/s channel occurs in M-Subframe n, in the n bit of the last set.

P2,	F1,	C1,	F2,	C2,	F3,	C3,	F4,	The C-bits of that M-Subframe are set to C1 = C2 = C3 = 1 if stuffing occurs.
M1,	F1,	C1,	F2,	C2,	F3,	C3,	F4,	C1 = C2 = C3 = 0 indicates no stuffing.
M2,	F1,	C1,	F2,	C2,	F3,	C3,	F4,	
M3,	F1,	C1,	F2,	C2,	F3,	C3,	F4,	TS = Test Sequence Bits.

The Stuff (justification) Block is structured as follows: (M1-SF to M7-SF indicate Subframes 1 to 7)

M1-SF	F4	Stuff bit 1	TS 590	TS 591	TS 592	TS 593	TS 594	TS 595	TS 596	.....	TS 672
M2-SF	F4	TS 589	Stuff bit 2	TS 591	TS 592	TS 593	TS 594	TS 595	TS 596	.....	TS 672
M3-SF	F4	TS 589	TS 590	Stuff bit 3	TS 592	TS 593	TS 594	TS 595	TS 596	.....	TS 672
M4-SF	F4	TS 589	TS 590	TS 591	Stuff bit 4	TS 593	TS 594	TS 595	TS 596	.....	TS 672
M5-SF	F4	TS 589	TS 590	TS 591	TS 592	Stuff bit 5	TS 594	TS 595	TS 596	.....	TS 672
M6-SF	F4	TS 589	TS 590	TS 591	TS 592	TS 593	Stuff bit 6	TS 595	TS 596	.....	TS 672
M7-SF	F4	TS 589	TS 590	TS 591	TS 592	TS 593	TS 594	Stuff bit 7	TS 596	.....	TS 672

6.9 Digital frames operating at bit rates of 97 728 kbit/s

In this case, the frame structure shall be as follows (see Recommendation G.752 [7]):

An M-frame comprises six sets (M-subframes) of 192 bits each and has a length of 1152 bits.

Set 1		Set 2		Set 3		Set 4		Set 5		Set 6	
M1	189 bits	M2	189 bits	M3	189 bits	M4	189 bits	M5	189 bits	M6	189 bits

The detailed structure of sets 1 to 3 is given below.

	M bits (bits 1-3)	Bits 4-192
Set 1	Frame Alignment Signal 1 1 0: $F_{11} = 1$, $F_{12} = 1$, $F_{13} = 0$	Test Sequence Bits 1-189
Set 2	Justification control bits: C_{11}, C_{21}, C_{31}	Test Sequence Bits 190-378
Set 3	Justification control bits: C_{12}, C_{22}, C_{32}	Test Sequence Bits 379-567
Set 4	Frame Alignment Signal 0 0 1: $F_{21} = 0$, $F_{22} = 0$, $F_{23} = 1$	Test Sequence Bits 568-756
Set 5	Justification control bits: C_{13}, C_{23}, C_{33}	Test Sequence Bits 757-945
Set 6	Auxiliary bits H_1 to H_3	Test Sequence Bits 946-1134 (Note)
TS Test Sequence Bits NOTE – The bit available for justification of each tributary is the first slot of that tributary following H_n. H_1 is the parity bit for the preceding frame, H_2 is reserved for national use, H_3 is used for Remote Alarm Indication (RAI).		

6.10 Digital frames operating at bit rates of 139 264 kbit/s

6.10.1 Digital frames operating at 139 264 kbit/s and multiplexing 34 368 kbit/s signals

In this case, the frame structure shall be as follows (see Recommendation G.751 [8]):

A frame comprises four sets of 488 bits each and has a length of 2928 bits.

Set 1		Sets 2 to 5		Set 6	
O1	472 bits	O2-5	484 bits	O6	484 bits

The detailed structure of sets 1 to 6 is given below.

	Overhead (O-) bits	Test Sequence Bits
Set 1	Frame Alignment Signal (bits 1 to 12): 1 1 1 1 1 0 1 0 0 0 0 0 Remote Alarm Indication (bit 13) Reserved for national use (bits 14-16)	Test Sequence Bits 1-472
Set 2-5	Justification control bits: C_{1n}, C_{2n}, C_{3n}, C_{4n}	Test Sequence Bits 473-2408
Set 6	Justification control bits: C_{15}, C_{25}, C_{35}, C_{45} Bits from tributaries available for justification (bits 5-8)	Test Sequence Bits 2409-2892 (2888)
NOTE – Concerning the use of stuffing (justification) bits see 6.1.1.		

6.10.2 Digital frames operating at 139 264 kbit/s and multiplexing 44 736 kbit/s signals

In this case, the frame structure shall be as follows (see Recommendation G.755 [14] and ANSI T1.107-1988 [11]):

An M-frame comprises six sets (M-subframes) of 159 bits each and has a length of 954 bits.

Set 1		Set 2		Set 3		Set 4		Set 5		Set 6	
M1	147 bits	M2	156 bits	M3	156 bits	M4	150 bits	M5	156 bits	M6	156 bits

The detailed structure of sets 1 to 3 is given below.

	M bits	Test Sequence Bits
Set 1	Frame Alignment Signal (bits 1-12): 1 1 1 1 1 0 1 0 0 0 0 0	Test Sequence Bits 1-147 (147 bits)
Set 2	Justification control bits: C_{11}, C_{21}, C_{31} (bits 1-3)	Test Sequence Bits 148-303 (156 bits)
Set 3	Justification control bits: C_{12}, C_{22}, C_{32} (bits 1-3)	Test Sequence Bits 304-459 (156 bits)
Set 4	Justification control bits: C_{13}, C_{23}, C_{33} (bits 1-3) Remote Alarm Indication (bit 4) Parity bit (bit 5) Reserved for future use (bits 6-9)	Test Sequence Bits 460-609 (150 bits)
Set 5	Justification control bits: C_{14}, C_{24}, C_{34} (bits 1-3)	Test Sequence Bits 610-765 (156 bits)
Set 6	Justification control bits: C_{15}, C_{25}, C_{35} (bits 1-3) Bits from tributaries available for justification (bits 4-6)	Test Sequence Bits 766-921/918 (156/153 bits)

6.11 Digital frames operating at STM-N bit rates

Test signal structures for measurements on SDH equipment operating at bit rates of 155 520 kbit/s, 622 080 kbit/s and 2 488 320 kbit/s can be found in Recommendation O.181.

7 Block-oriented error performance measurements

7.1 Measurement of block errors

Recommendation G.826 defines error performance parameters and objectives applicable to digital paths operating at or above the primary rate. The Recommendation requires that error performance measurements are based upon the evaluation of blocks.

Measurement instrumentation intended to perform error measurements conforming to Recommendation G.826 shall also adhere to the block-based concept. In this case, measurement results will be obtained in the form of block errors or block error ratios.

However, this requirement does not preclude the optional measurement and evaluation of single bit errors resulting in bit errors or bit error ratios.

7.2 Block sizes

In order to obtain compatible measurement results, block-oriented error performance measurements need to be based on identical block sizes.

7.2.1 Block sizes for out-of-service performance measurements on PDH systems

Recommendation G.826 [5] defines block sizes for in-service measurements at bit rates at which inherent Error Detection Codes (EDC) are in use. These block sizes shall also be used for out-of-service measurements. (See Table 2).

TABLE 2/O.150

Block Sizes for PDH Error Performance Monitoring with EDC

Bit Rate	PDH Block Size	PDH Block Length	Basis	References
1544 kbit/s	4632 bits	3 ms	CRC-6	2.1/G.704 Annex B/G.826
2048 kbit/s	2048 bits	1 ms	CRC-4	2.3/G.704 Annex B/G.826
6312 kbit/s	3156 bits	500 µs	CRC-5	2.2/G.704 Annex B/G.826
44 736 kbit/s	4760 bits	106 µs	Single Bit Parity Check	1.3/G.752 Annex B/G.826

For measurements at bit rates where no EDC exists, the preferred optional block sizes are given in Table 3.

TABLE 3/O.150

Block Sizes for PDH Error Performance Monitoring without EDC

Bit Rate	PDH Block Size	PDH Block Length	Basis
8448 kbit/s	4224 bits	500 µs	(No EDC, see Note)
32 064 kbit/s	4008 bits	125 µs	(No EDC, see Note)
34 368 kbit/s	4296 bits	125 µs	(No EDC, see Note)
97 728 kbit/s	12 216 bits	125 µs	(No EDC, see Note)
139 264 kbit/s	17 408 bits	125 µs	(No EDC, see Note)
NOTE – Where reference is made to an Error Detection Code (EDC), the block size is given by the EDC mechanism. Where no EDC is defined, the block size is based upon multiples of 125 µs. The actual block size/block length may deviate from the nominal value given in the table by ± 5 %.			

7.2.2 Block sizes for out-of-service performance measurements on SDH systems

Table 4 gives block sizes for error performance measurements of SDH paths. These block sizes are defined in Recommendation G.826 for in-service measurements and shall also be used for out-of-service measurements.

Block sizes for measurements at multiplex sections, can be found in relevant G-Series error performance Recommendations.

TABLE 4/O.150

Block Sizes for SDH Error Performance Monitoring

Bit Rate of Path	SDH Path Size	SDH Block Size	EDC (Note)	References
1664 kbit/s	VC-11	832 bits	BIP-2	Annex C/G.826
2240 kbit/s	VC-12	1120 bits	BIP-2	Annex C/G.826
6848 kbit/s	VC-2	3424 bits	BIP-2	Annex C/G.826
48 960 kbit/s	VC-3	6120 bits	BIP-8	Annex C/G.826
150 336 kbit/s	VC-4	18 792 bits	BIP-8	Annex C/G.826
34 240 kbit/s	VC-2-5c	17 120 bits	BIP-2	Annex C/G.826
601 344 000 kbit/s	VC-4-4c	75 168 bits	BIP-8	Annex C/G.826
NOTE – The block size is based upon the inherent SDH Error Detection Code (EDC).				

7.2.3 Block sizes for performance measurements on cell-based systems

Block sizes for performance measurements on cell-based systems are defined in Recommendation O.191.

8 Detection and clearance of AIS and LOS defects

Measurement instrumentation specified in the O-Series Recommendations which is intended to operate at digital interfaces, e.g. at interfaces in accordance with Recommendation G.703 [9], may be required to monitor the status of the signal to be evaluated. The Alarm Indication Signal (AIS) and Loss Of Signal (LOS) are examples of such defects.

The criteria for the detection and clearance of LOS and AIS defects at interfaces operating at bit rates conforming to Recommendation G.703 are given in Recommendation G.775 [10] and shall be observed by O-Series instrumentation.

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